

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	8	("5778439") or ("5760602") or ("5036473") or ("5109353") or ("5140526") or ("5430687") or ("5500609") or ("5504440")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:08
S51	237	712/10.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S52	186	712/37.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S53	721	712/227.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S54	106	FPGA and ("shift register" same circular)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S55	1	FPGA and ("shift register" same circular same clb)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S56	57	S54 and selector	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S57	184	("4642487" "4700187" "4703435" "4706216" "4722084" "4724307" "4744084" "4758985" "4768196" "4786904" "4815003" "4829202" "4849928" "4868419" "4908772" "4935734" "4949275").PN. OR ("5036473").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/02 13:08
S58	67	S57 and "shift register"	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/02 13:08
S59	1351	(326/39).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:08
S60	752	S59 and fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S61	1	tremblay.in. and fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S62	80	tremblay.in. and programmable	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S63	35	(fpga or "programmable logic") and ((cache or cached or time-multiplexed or paged or overlay) same CLB)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S64	128	"time-multiplexed" same (fpga or "programmable logic")	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S65	5	paged same (fpga or "programmable logic")	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S66	25	"dynamically reconfigurable fpga"	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08

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S67	1	("5,646,545").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:09
S68	33	overlay with fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S69	329	partition\$2 with fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S70	54	partition\$2 with clb	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S71	9	selecting near2 CLB	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S72	20	S70 and selector	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S73	32	S70 and (CLB same multiplex\$2)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S74	54	partition\$2 with clb	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S75	20	S74 and selector	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S76	237	712/10.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S77	106	FPGA and ("shift register" same circular)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S78	186	712/37.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S79	32	S74 and (CLB same multiplex\$2)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S80	184	("4642487" "4700187" "4703435" "4706216" "4722084" "4724307" "4744084" "4758985" "4768196" "4786904" "4815003" "4829202" "4849928" "4868419" "4908772" "4935734" "4949275").PN. OR ("5036473").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/02 13:08
S81	128	"time-multiplexed" same (fpga or "programmable logic")	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S82	67	S80 and "shift register"	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/02 13:08
S83	25	"dynamically reconfigurable fpga"	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S84	329	partition\$2 with fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S85	1351	(326/39).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:09

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S86	1	tremblay.in. and fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:09
S87	57	S77 and selector	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S88	80	tremblay.in. and programmable	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S89	35	(fpga or "programmable logic") and ((cache or cached or time-multiplexed or paged or overlay) same CLB)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S90	8	(("5778439") or ("5760602") or ("5036473") or ("5109353") or ("5140526") or ("5430687") or ("5500609") or ("5504440")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:08
S91	1	("5,646,545").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/10/02 13:08
S92	33	overlay with fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S93	752	S85 and fpga	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S94	5	paged same (fpga or "programmable logic")	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S95	9	selecting near2 CLB	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S96	1	FPGA and ("shift register" same circular same clb)	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08
S97	721	712/227.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:08